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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,219	09/26/2003	Naotaka Yumoto	030712-14	6834

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/670,219	YUMOTO, NAOTAKA	
	Examiner	Art Unit	
	Jung (John) H. Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *6-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 31 October 2007 has been entered.

Amendment

2. Acknowledgment is made of applicant's Amendment, filed 31 October 2007. The changes and remarks disclosed therein have been considered.

No claim has been cancelled or added by Amendment. Therefore, claims 1-29 remain pending in the application.

Election/Restrictions

3. Claims 6-20 remain withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11 February 2005.

Specification

4. Claims 1, 21 and 29 are objected to because of the following informalities:

In claims 1, 21 and 29, "the voltage" in the amended portion is understood as --a voltage--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-5, 21, 23-26, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art ("APA") in view of Rozman (U.S. Pat. No. 5,177,745), McGibney et al. (U.S. Pat. No. 6,112,322) and McClure (U.S. Pat. No. 6,037,792).

APA (for example, in the second paragraph on page 1 of the specification) discloses a nonvolatile semiconductor memory device comprising: a memory cell array having a plurality of memory cells and arranged in an array, the memory cells being connected to a plurality of bit lines and word lines (inherent); a plurality of address input terminals inputting a plurality of addresses thereto (inherent); a test mode circuit for outputting a test mode signal (implied, for example, to control the operations of column switches) according to a predetermined voltage (associated with "a signal from the exterior") to a predetermined terminal (implied, since the signal is from the exterior) when a signal ("a signal from the exterior") is inputted to the predetermined terminal; a row decoder (inherent); applying an excess voltage ("a test mode voltage" of 8V, above the normal level of 5V) for a test to all said word lines in response to said test mode signal; a column decoder (including "column switches") connected to said test mode circuit and setting all said bit lines to a non-selecting state ("a turning-off state") in response to

said test mode signal; a control signal input terminal for receiving a control signal (inherent; such as RAS, CAS, R/W, etc.) and a control circuit connected to this control signal input terminal (inherent, for example, to control read/write operations); and an address buffer connected to the address input terminals, the row decoder and the column decoder (inherent).

However, APA does not expressly disclose that the predetermined terminal is that among or of the plurality of address input terminals; said test mode circuit operatively connected to inhibit a voltage to a selected memory cell via the test mode signal; and a monitor terminal (or pad) connected to said test mode circuit, said monitor terminal outputting said test mode signal for confirming a test mode. Further, APA is not clear that said row decoder is connected to said test mode circuit, said test mode signal being inputted to said row decoder for applying said excess voltage to all said word lines.

Rozman discloses use of a predetermined terminal among or of a plurality of address input terminals to enter or enable a test mode (see for example column 2, lines 13-17 and column 5, lines 1-3).

McClure, for example in Figs. 1 and 3, discloses a monitor terminal or pad (48 or 54 or 72) for outputting a test mode signal (for example, /BURN-IN MODE signal in Fig. 1 or /TEST MODE signal in Fig. 3, via 52 and 50) for confirming a test mode (see for example column 3, lines 35-40, column 5, lines 37-52, and column 6, lines 56-61).

McGibney, for example in Fig. 4, discloses a test mode signal (404) being inputted to a row decoder (402, along with 403 to accommodate the test mode) for applying an excess voltage (above VCC; see for example column 2, lines 10-15, column 4, lines 47-56) to all word lines (see for example column 2, line 60 through column 3, lines 10).

Since it was common and well known in the art to detect a predetermined signal on an existing address pin to enable a test mode (as exemplified by Rozman), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to enable the test mode of APA via a signal on a predetermined terminal among or of the plurality of address input terminals, for the purpose of reducing the need for additional pins to enable a test mode and thus reducing the space and cost associated with providing additional pins (see for example Rozman column 2, lines 63-66).

Further, since APA's memory cells are not in a normal read/write/erase operation during the stress test (see APA), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have said test mode circuit operatively connected to inhibit a voltage to a selected memory cell (i.e., inhibit a normal operating voltage commonly applied to a selected memory cell during a normal read/write/erase operation) via the test mode signal and apply instead an appropriate stress test voltage(s), for the purpose of creating an optimum condition for effectively and efficiently conducting the stress test (see APA).

Further, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate a test mode monitor terminal (or pad), as in McClure, in the test mode circuit of APA, for the purpose of ascertaining (or confirming) a test mode entry and exit and thus reducing test errors and increasing test quality (see also for example McClure, column 5, lines 40-44).

Further, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have the row decoder connected to the test mode circuit of APA such that the row decoder would select and apply the excess voltage to all the word lines

(as in McGibney), for the purpose of providing a greater flexibility for stress testing by being able to control the selection of the word lines, while preventing power surges (see for example McGibney column 2, line 47 through column 3, line 14).

7. Claims 2, 22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art ("APA") in view of Rozman, McGibney et al. and McClure as applied to claims 1, 21 and 26 above, and further in view of Fontana et al. (U.S. Pat. No. 5,982,677).

The above APA/Rozman/McGibney/McClure combination discloses a memory device as in claims 1, 21 and 26 above, with the exception of a select line connected to the drain of a memory cell, and a regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

Fontana, for example in Figs. 2 and 3, discloses a select line (Yms) connected to the drain of a memory cell (see 3 in Fig. 2), and a regulator (Fig. 3) connected to this select line and a circuit (providing Vref and PGn), and giving a predetermined bias electric potential to the drain of said memory cell (see for example column 4, lines 26-37).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include a drain voltage regulator, as in Fontana, in the device of the APA/Rozman/McGibney/McClure combination to provide a voltage to the drains of the memory cells, for the purpose of stabilizing the drain voltage during programming of multiple memory cells (see for example Fontana, column 3, lines 37-41), and connect the regulator to the test mode circuit, for the purpose of flexibly controlling the regulator during a test mode (for example, to enable/disable/adjust the regulator voltage for testing).

Response to Arguments

8. Applicant's other arguments filed 31 October 2007 have been fully considered but they are not persuasive.

In response to Applicant's argument, in the intervening paragraph between pages 12 and 13 of Remarks, it is noted that the combination of APA, Rozman, McGibney and McClure does suggest a test mode circuit operatively connected to inhibit a voltage to a selected memory cell via the test mode signal. See the rejections above.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) H. Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

/J. H. Hur/
Primary Patent Examiner
Art Unit 2824
27 December 2007